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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,994	10/17/2001	Makoto Nagata	50006-128	4496

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EXAMINER

WEST, JEFFREY R

ART UNIT	PAPER NUMBER
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2857

DATE MAILED: 05/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/977,994

Applicant(s)

NAGATA ET AL.

Examiner

Jeffrey R. West

Art Unit

2857

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 02/19/04
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

1. Claims 2, 3, 5, 7, 9, 10, and 12 are objected to because of the following informalities.

To avoid problems with antecedent basis:

In claim 2, line 2, and claim 9, line 2, "segments along the border" should be ---segments along a border---.

In claim 3, line 3, and claim 10, line 3, "wherein the length" should be ---wherein a length---.

In claim 5, lines 1-2, and claim 12, lines 1-2, "wherein capacitance of the parasitic capacitor to be charged" should be ---wherein a capacitance of the parasitic capacitors to be charged at a specific timing---.

In claim 7, line 3, "receiving the design specification" should be ---receiving a design specification---.

In claim 7, line 8, "reviewing the result" should be ---reviewing a result---.

In claim 9, lines 4-5, "statically charged" should be ---charged statically---.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-6 and 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata et al., "Measurements and Analyses of Substrate Noise Waveform in Mixed Signal IC Environment" in view of U.S. Patent Application Publication No. 2002/0022951 to Heijningen et al.

Nagata discloses a method for performing measurements and analyses of substrate noise waveform in mixed signal integrated circuit environment comprising representing the integrated circuit according to a distribution of switching operations of a plurality of logic gates and a time series of statically-charged parasitic capacitors connected between a source line and a ground line (page 577, column 1, paragraph 5 and Figure 7). Nagata then discloses generating an analysis module by coupling one end of the group of capacitors with a parasitic impedance of the source line, and connecting the other end of the group of capacitors with a parasitic impedance of the ground line (Figure 7). Nagata also discloses that the source current from the analysis model along with the parasitic impedances of the source and ground lines causes a voltage variation, regarded as substrate noise (page 576, column 1, paragraph 3, page 577, column 1, paragraph 4, and Figure 5). Nagata further discloses that a value for the parasitic capacitances is determined every predetermined time interval wherein the time interval is set according to the switching operations of the logic gates (page 577, column 2, paragraph 2 to page 578, column 2, paragraph 2). Also, although not specifically disclosed, it is

considered inherent that the time interval is shorter as the frequency of the switching operations is greater since frequency and time have an inverse relationship.

With respect to claims 2 and 9, Nagata discloses assigning the group of parasitic capacitors to a group of logic gates wherein the digital circuit is divided into a plurality of segments along the border at which the parasitic impedances of the source line and the ground line are locally appended (i.e. increased) (Figures 7a-c and page 577, column 2, paragraph 2).

With respect to claims 5 and 12, Nagata discloses that the capacitor groups are charged at a specific timing according to the output of a truth table (page 277, column 1, paragraph 5) wherein capacitance of the parasitic capacitor to be charged is calculated from input and output capacitance of the logic gates in the digital circuit to be analyzed (page 577, column 2, paragraph 2 and equation (2)) (input capacitances, $C_{in,i}$ and $C_{ip,j}$, and output capacitances $C_{jn,i}$ and $C_{jp,j}$).

Nagata, however, presents the voltage variation as a measure of noise and doesn't specifically disclose determining the waveform of the source current in the digital circuit from the analysis model. Nagata is also silent on whether the parasitic capacitors are a time-series group of parasitic capacitors.

Heijningen teaches a method, apparatus and computer program product for determination of noise in mixed signal systems caused by the switching operation of logic gates on a substrate (0007-0008) including representing the logic gate switching as capacitor groups in the form of a cell (0088, lines 1-5) and determining the noise as a source current waveform (0089) wherein determining the power

supply noise requires determining a capacitance contribution for each cell (i.e. capacitor group) independently (i.e. time division groups) (0119) and combining the individual waveforms to determine the total noise waveform (0127).

It would have been obvious to one having ordinary skill in the art to modify the invention of Nagata to include determining the waveform of the source current in the digital circuit from the analysis model and specifying that the parasitic capacitors be a time-series group of parasitic capacitors, as taught by Heijningen, because Nagata does teach determining the noise as represented by voltage waveforms as well as that the capacitor groups are charged at a specific timing according to the output of a truth table and, as suggested by Heijningen, the combination would have provided a method for correctly determining the effect of the capacitances (0088, lines 18-28), a simplified substrate and gate model based substrate voltage profile using a current profile (0089, lines 7-21), and a corresponding method for obtaining the power supply waveform by determining the effect of each group individually and then combining the waveforms of each group (0119 and 0127) in order to quickly and accurately determine the noise in a system having a large amount of gates (0087).

Further, Applicant admits as well known in the art, in the Background of the Invention, that "the principal cause of substrate noise generation is a change in voltage generated when the source current of the digital circuits flowing through internal power-supply and ground wirings, which connect the external power supply to the LSI chip, interacts with the parasitic impedances parasitic on those wirings" (page 2, lines 15-20) and "As clearly understood, the generation of noises largely

depends on a change in the source current" (page 3, lines 1-2). Therefore, it would have been obvious to one having ordinary skill in the art to specify that the source current waveform be determined from a source current waveform because the combination would have allowed for the analysis of the most likely representation of noises. *When applicant states that something is prior art, it is taken as being available as prior art against the claims. Admitted prior art can be used in obviousness rejections. In re Nomiya, 509 F.2d 566, 184 USPQ 607, 610 (CCPA 1975).*

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata et al. in view of Heijningen and further in view of Mitra et al., "Substrate-Aware Mixed Signal Macrocell Placement in WRIGHT".

As noted above, the invention of Nagata and Heijningen teaches many of the features of the claimed invention including using the method during the circuit design stage (Heijningen, 0079), but does not specifically disclose the method for designing the semiconductor integrated circuit comprising receiving the design information, designing analog and digital circuit according to the design specifications, and re-designing the analog and digital circuits or their layout and the location of guard bands by reviewing the result of substrate noise analysis.

Mitra teaches a computer-implemented method for handling substrate-coupled switching noise in a typical IC containing both sensitive analog and noisy digital circuits (abstract) comprising first receiving minimal area and wire length design

specifications, designing the circuits based on the design specifications, and from the design determining the current substrate noise. Mitra then teaches re-designing, based on the substrate noise results, the circuits and guard ring/band positions to obtain acceptable substrate noise results (page 275, column 2, paragraph 3 to page 276, column 1, paragraph 3).

It would have been obvious to one having ordinary skill in the art to modify the invention of Nagata and Heijningen to include a method for designing the semiconductor integrated circuit comprising receiving the design information, designing analog and digital circuit according to the design specifications, and re-designing the analog and digital circuits or their layout and the location of guard bands by reviewing the result of substrate noise analysis, as taught by Mitra, because, as suggested by Mitra, the combination would have provided a method for incorporating a simplified switching noise estimation into a simulated annealing placement algorithm to allow substrate design that can be used during the design wherein efficient evaluation is critical, but much information about the final chip remains unavailable (page 277, column 1).

Response to Arguments

5. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

The Examiner does note, however, that the affidavits filed 37 CFR 1.132 are sufficient to eliminate Nagata et al., "Physical Design Guides for Substrate Noise Reduction in CMOS Digital Circuits" as prior art.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure:

U.S. Patent No. 6,144,217 to Iwata et al. teaches a low switching noise logic circuit including a plurality of switching capacitors.

U.S. Patent No. 4,366,456 to Ueno et al. teaches a switched-capacitor filter including a plurality of time-division capacitor groups.

U.S. Patent No. 4,543,546 to Hariharan teaches a switched capacitor circuit with minimized switched capacitance including a plurality of time-division capacitor groups for representing resistive circuit elements.

U.S. Patent No. 5,424,670 to Samuels et al. teaches a precision-switched capacitor ratio system including a switching device for selectively interconnecting a capacitor with one of a plurality of charging circuits at specific timings.

7. If a copy of a provisional application listed on the bottom portion of the accompanying Notice of References Cited (PTO-892) form is not included with this Office action and the PTO-892 has been annotated to indicate that the copy was not readily available, it is because the copy could not be readily obtained when the

Office action was mailed. Should applicant desire a copy of such a provisional application, applicant should promptly request the copy from the Office of Public Records (OPR) in accordance with 37 CFR 1.14(a)(1)(iv), paying the required fee under 37 CFR 1.19(b)(1). If a copy is ordered from OPR, the shortened statutory period for reply to this Office action will not be reset under MPEP § 710.06 unless applicant can demonstrate a substantial delay by the Office in fulfilling the order for the copy of the provisional application. Where the applicant has been notified on the PTO-892 that a copy of the provisional application is not readily available, the provision of MPEP § 707.05(a) that a copy of the cited reference will be automatically furnished without charge does not apply.


8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (703)308-1309. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7382 for regular communications and (703)308-7382 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

jr
May 14, 2004


MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800